

WHAT IS CLAIMED IS:

- 1 1. A method of providing self-aligning features on a semiconductor device comprising the
2 steps of:
 - 3 providing a substrate with a dielectric layer that defines at least one line of metallization;
 - 4 recessing the top surface of said at least one line of metallization below the top surface of
 - 5 said dielectric layer;
 - 6 capping said at least one line of metallization with a barrier layer deposited over the top
 - 7 surface of said substrate, said barrier layer defining a top surface that follows the contours of the
 - 8 top surface of said at least one line of metallization and said dielectric;
 - 9 depositing a layer of liner material over said barrier layer, said layer also following the
 - 10 contours of said at least one line of metallization and said dielectric;
 - 11 planarizing said layer of liner material so as to remove high areas such that the low areas
 - 12 of said liner material remain; and
 - 13 etching selected features in said dielectric layer of said substrate by using said remaining
 - 14 low areas of said liner material as a hard mask.
- 1 2. The method of claim 1 wherein said barrier layer is selected from silicon nitride and
- 2 silicon carbide.
- 1 3. The method of claim 1 further comprising the step of depositing an ILD (intermediate
- 2 layer dielectric) layer over said capping layer before depositing said layer of liner material.

1 4. The method of claim 1 wherein said layer of liner material is selected from the group
2 consisting of Tantalum (Ta), Tantalum Nitride (TaN), Titanium (Ti), Titanium Nitride (TiN),
3 Silicon Nitride (SiN), and Silicon Carbide (SiC).

1 5. The method of claim 1 wherein substrate defines at least two spaced apart lines of
2 metallization such that said hard mask defines unmasked areas between said two lines of
3 metallization and said selected etched feature is a via.

1 6. The method of claim 1 wherein said step of providing comprises the step of providing a
2 substrate with at least one trench defined therein, depositing a barrier liner over said at least one
3 trench and the top surface of said dielectric, and depositing a conductive material over said
4 substrate so as to fill said at least one trench and cover said substrate.

1 7. The method of claim 6 wherein said conductive material is a metal selected from the
2 group consisting of copper and aluminum.

1 8. The method of claim 6 further comprising planarizing said deposited conductive material
2 by a method selective to said barrier liner so as to remove said conductive material down to said
3 barrier liner.

1 9. The method of claim 8 further comprising the step of polishing said substrate to remove
2 said barrier liner covering said dielectric.

1 10. The method of claim 9 wherein said recessing step comprises the step of polishing said
2 substrate with a material selective to said dielectric layer of said substrate such that said at least
3 one line of metallization is recessed below the top surface of said dielectric.

1 11. The method of claim 1 wherein said recessing step comprises the step of polishing said
2 substrate with a CMP (chemical-mechanical polishing) material selected to said dielectric layer
3 of said substrate such that said at least one line of metallization is recessed below the top surface
4 of said dielectric.

1 12. The method of claim 1 wherein said recessing step comprises the step of etching said
2 conductive material selective to said dielectric material.

1 13. The method of claim 10 further comprising the step of depositing an ILD layer over said
2 capping layer before depositing said layer of liner material.

1 14. The method of claim 10 wherein said layer of liner material is selected from the group
2 consisting of, Tantalum (Ta), Tantalum Nitride (TaN), Titanium (Ti), Titanium Nitride (TiN),
3 Silicon Nitride (SiN), and Silicon Carbide (SiC).

1 15. The method of claim 10 wherein said substrate defines at least two spaced apart lines of
2 metallization such that said hard mask defines unmasked areas between said two lines of
3 metallization and said selected etched feature is a via.

1 16. The method of claim 1 wherein said feature etched in said dielectric layer is a trench.

1 17. The method of claim 11 further comprising the step of depositing an ILD layer of said
2 capping layer before depositing said layer of liner material.

1 18. The method of claim 11 wherein said layer of liner material is selected from the group
2 consisting of, Tantalum (Ta), Tantalum Nitride (Ta_N), Titanium (Ti), Titanium Nitride (Ti_N),
3 Silicon Nitride (Si_N), and Silicon Carbide (SiC).

1 19. The method of claim 11 wherein said substrate defines at least two spaced apart lines of
2 metallization such that said hard mask defines unmasked areas between said two lines of
3 metallization and said selected etch feature is a via.